The following listing of Claims replaces all previous listings:

1. (Original) A method of forming a metal-insulator-metal type capacitor structure in an integrated circuit memory device, comprising:

crystallizing an HfO_2 dielectric layer on a lower electrode of a capacitor structure in a low temperature plasma treatment at a temperature in a range between about 250 degrees Centigrade and about 450 degrees Centigrade; and

forming an upper electrode on the HfO_2 dielectric layer.

2. (Original) A method according to Claim 1 wherein crystallizing an HfO_2 dielectric layer further comprises:

crystallizing the HfO_2 dielectric layer in a range between about 350 degrees Centigrade and about 450 degrees Centigrade.

3. (Original) A method according to Claim 1 wherein forming an upper electrode comprises forming the upper electrode using a metal source containing halogen or an organometallic compound, or a combination thereof.

4. (Original) A method according to Claim 3 wherein forming the upper electrode using a metal source further comprises forming the upper electrode using a metal source containing Cl.

5. (Currently amended) A method according to Claim 1 wherein crystallizing an HfO_2 dielectric layer further comprises:

crystallizing the HfO_2 <u>dielectric</u> layer in the low temperature plasma atmosphere including an N gas.

6. (Currently amended) A method according to Claim 5 wherein crystallizing an HfO_2 dielectric layer further comprises:

crystallizing the HfO_2 <u>dielectric</u> layer in the low temperature plasma atmosphere including NH_3 gas or N_2O gas or [[N_2,]] <u>N_2</u> gas or combinations thereof.

7. (Currently amended) A method of forming a metal-insulator-metal type capacitor structure in an integrated circuit memory device, comprising:

forming a lower electrode on a substrate;

forming an HfO_2 dielectric layer on the lower electrode;

processing the HfO_2 dielectric layer in a plasma atmosphere at a temperature in a range between about 250 degrees Centigrade and about 450 degrees Centigrade; and

forming an upper electrode on the HfO_2 dielectric layer.

8. (Original) A method according to Claim 7 wherein the lower electrode is formed of a metal nitride or a noble metal or combinations thereof.

9. (Original) A method according to Claim 8 wherein the lower electrode is formed of TiN or TaN or WN or Ru or Ir or Pt or combinations thereof.

10. (Original) A method according to Claim 7 wherein the HfO_2 dielectric layer is formed using atomic layer deposition or chemical vapor deposition or physical vapor deposition or metal-organic chemical vapor deposition.

11. (Presently amended) A method according to Claim 7 wherein processing the HfO_2 dielectric layer in a plasma atmosphere is performed using plasma of N-containing gas.

12. (Currently Amended) A method according to Claim 11 wherein the N-containing gas includes ~~NH3 or N2O or N2~~ NH_3 or N_2O or N_2 or combinations thereof.

13. (Original) A method according to Claim 7 wherein the upper electrode is formed of a metal nitride or a noble metal or combinations thereof.

14. (Original) A method according to Claim 13 wherein the upper electrode is formed of TiN or TaN or WN or Ru or Ir or Pt, or combinations thereof.

15. (Original) A method according to Claim 7 wherein the upper electrode is formed using a halogen-containing metal source or an organometallic compound source or a combination thereof.

16. (Original) A method according to Claim 7 wherein the lower electrode has a one-cylinder-stack (OCS) structure.

17. (Original) A method according to Claim 7 wherein the plasma atmosphere is maintained at a temperature in a range between about 250 degrees Centigrade and about 450 degrees Centigrade.

18. (Currently amended) A method of forming a metal-insulator-metal type capacitor in an integrated circuit memory device, comprising:

forming a buried contact plug in a first interlayer dielectric layer on a substrate;

forming a silicon nitride layer and a second interlayer dielectric layer on the buried contact plug;

forming a buffer buried contact plug in the silicon nitride layer and in the second interlayer dielectric layer to contact the buried contact plug;

sequentially forming a high density plasma layer, a silicon nitride layer, a protection layer, and an insulating layer on the buffer buried contact plug to form a cover layer;

removing a portion of the cover layer to form a hole to expose at least a portion of the buffer buried contact plug;

forming a conductive layer in the hole and outside the hole on the insulating layer using a Cl source metal;

forming a sacrificial layer on the conductive layer inside and outside the hole;

removing a portion of the of the sacrificial layer outside the hole to expose the insulating layer;

removing the insulating layer from around the conductive layer to form a lower electrode for the capacitor;

forming an amorphous HfO_2 dielectric layer on the lower electrode;

crystallizing the amorphous HfO_2 dielectric layer on the lower electrode in a low temperature plasma atmosphere including NH_3 gas or N_2O gas or [[N_2,]] $\underline{N_2}$ gas or combinations thereof in temperature range between about 350 degrees Centigrade and about 450 degrees Centigrade to provide a crystallized HfO_2 dielectric layer; and

forming an upper electrode on the crystallized HfO_2 dielectric layer using a halogen-containing metal source or an organometallic compound source or a combination thereof.

19. (New) A method of forming a metal-insulator-metal type capacitor structure in an integrated circuit memory device, comprising:

crystallizing an existing HfO_2 dielectric layer on a lower electrode of a capacitor structure in a plasma atmosphere at a temperature in a range between about 250 degrees Centigrade and about 450 degrees Centigrade; and

forming an upper electrode on the HfO_2 dielectric layer.

20. (New) A method according to Claim 19 further comprising:

forming the HfO_2 dielectric layer using Atomic Layer Deposition (ALD) prior to crystallizing.